Docket: P910328

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Yi Chou Chen

U.S. Serial No: 10/802,312

Filed: March 17, 2004

For: METHOD OF FORMING A CHALCOGENIDE MEMORY CELL HAVING A HORIZONTAL ELECTRODE AND A MEMORY CELL PRODUCED BY THE METHOD

Examiner: Fenty, Jesse A

Group Art: 2815

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION UNDER 37 C.F.R. 1.131

I, Yi Chou Chen, declare as follows:

1. I am the inventor of the claims of the above-identified patent application.

2. Prior to December 13, 2002, I conceived the invention of forming a chalcogenide memory cell having a horizontal electrode, with a small cross-sectional area that makes electrical contact with a chalcogenide memory element, to thereby form the memory cell, as described and claimed in the referenced application.

3. A document illustrating my idea, prepared by me before December 13, 2002, is attached as Exhibit A. I prepared another document, prior to December 13, 2002, and had it transmitted to one of Macronix' s patent law firms, Stout, Uxa, Buyan & Mullins, LLP, with a request and authorization that a U.S. patent application be prepared and filed on the material described in the other document. A copy of this other document is attached hereto as Exhibit B.

4. A patent application was subsequently prepared and filed by the law firm in the U.S. Patent and Trademark Office.

The below undersigned declares that all statements made of his own knowledge are true and that all statements made on information and belief are believed to be true, being duly warned that willful false statements and the like are punishable by fine or imprisonment, or both, (18 U.S.C. 1001) and may jeopardize the validity of the application or any patent issuing therefrom.

2/27/06
Date

Yi-Chou, Chen
Yi Chou Chen

APPENDIX A

MXIC 旺宏電子 MACRONIX INTERNATIONAL

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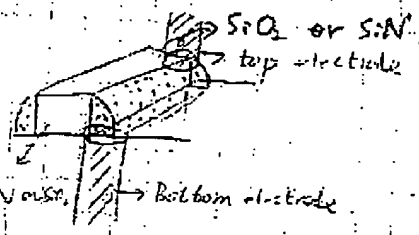
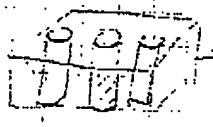
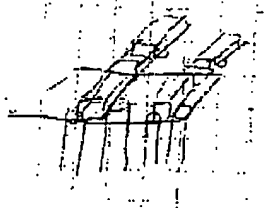
工作名稱： Super small Ultra cross-section chalcogen 4 cell

Structure :

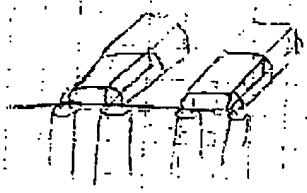


Process : 1. Bottom electrode 2 (SiN/SiO_2) Dep / Photo / Etch

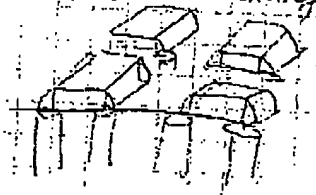




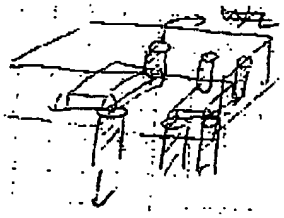
3. chalcogenide Dep / EB.



3.5 /Etching Photo to cut the SiN and chalcogenide



4. OXIDE/SiN Dep / Top electrode Photo / Etch

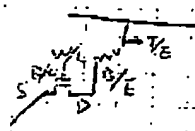


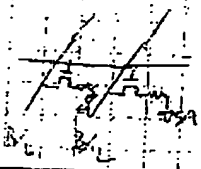
/ Top electrode Dep.

(CVD poly)

Transistor or P-N Diode

Circuit :





記錄人： 何家騰	日期： [redacted]	見證人： 何家騰	日期： [redacted]

報告之 [redacted]

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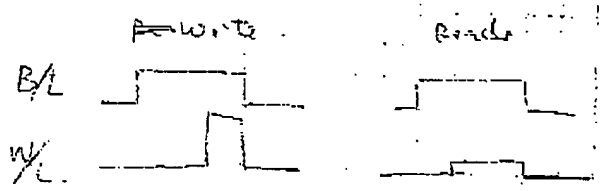
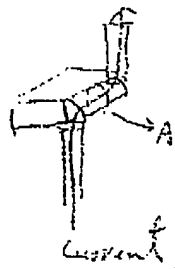
工作名稱： continue

Operation :





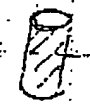
Pros. ① The cross section of the chalcogenide is Vitra small.

eg. Si:N thickness = 1000Å

chalcogenide thickness = 2000Å

Then the Area = 1000Å × 2000Å = 2E5 Å²

If chalcogenide is in a contact



the diameter of the contact is

$\frac{\pi}{4} D^2 = 2E5$

$D = 504 Å \sim 0.05 \mu m$

It's too difficult !!!

for ~~248 or 193~~ the

but using this tech. The limitation is no longer exist!

The diameter is determined by film thickness

記錄人： 陳逸舟	日期： [redacted]	見證人： 何家瑋	日期： [redacted]
		賴再志	[redacted]

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工作名稱：Utra small cross-section electrode in chalcogenide memory

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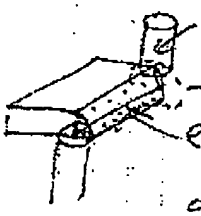
Relacing the chalcogenide by Metal / electrode in the previous invention. And we can get a Utra small cross-sectional area in the electrode



chalcogenide → small active area

electrode with ultra small cross-section area

記錄人：[redacted] 日期：[redacted] 見證人：[redacted] 日期：[redacted]

APPENDIX B

P910328

TITLE OF INVENTION

Definition of the contact area of electrode and phase change material in the chalcogenide phase-change memory

[redacted]

CLASSIFICATION : Method

SUITABLE PRODUCT : Chalcogenide Memory (Next generation memory)

(This page will be provided by IPO)

BACKGROUND OF THE INVENTION

☐ Field of the invention

- The invention describes a innovational method to fabricate ultra small contact area between electrode and phase change material in the chalcogenide phase change memory. With this method, the contact area of the chalcogenide part and electrode will be ultra small, and as a result the current/power requirement of the chalcogenide memory dramatically decrease. The contact area of the chalcogenide part and electrode is defined by the thin film process and etching process in this invention.

☐ The issues were solved and improvement by the invention

- It is known that the chalcogenide phase change memory is not easy to be driven by CMOS circuit, because chalcogenide requires relatively high current to change its phase. Reducing the cross-sectional area of chalcogenide or electrode can reduce the current requirement directly. Many structures has been invented to reduce area. For example, to fabricate a ultra small contact hole and place the chalcogenide into the contact. However, these inventions basically are limited by lithography. Furthermore, it is very difficult to place materials into ultra small and deep holes. In this invention, contact area of the chalcogenide part and electrode is defined by the thin film process and etching process. Therefore, the lithography is no longer the limit. It is also not necessary to place materials into ultra small holes. Moreover, contact area of the chalcogenide part and electrode is ultra small. As a result, the current/power requirement of the chalcogenide memory is dramatically decreased.

SUMMARY OF THE INVENTION

- How this invention solves existing problems and achieves the objects
- The contact area of the chalcogenide part and electrode is defined by 1. electrode film thickness and 2. The thickness of pad layer. With well control of film thickness, the area will be very small. Therefore the current required in the chalcogenide phase-change memory is reduced.

BRIEF DESCRIPTION OF DRAWING

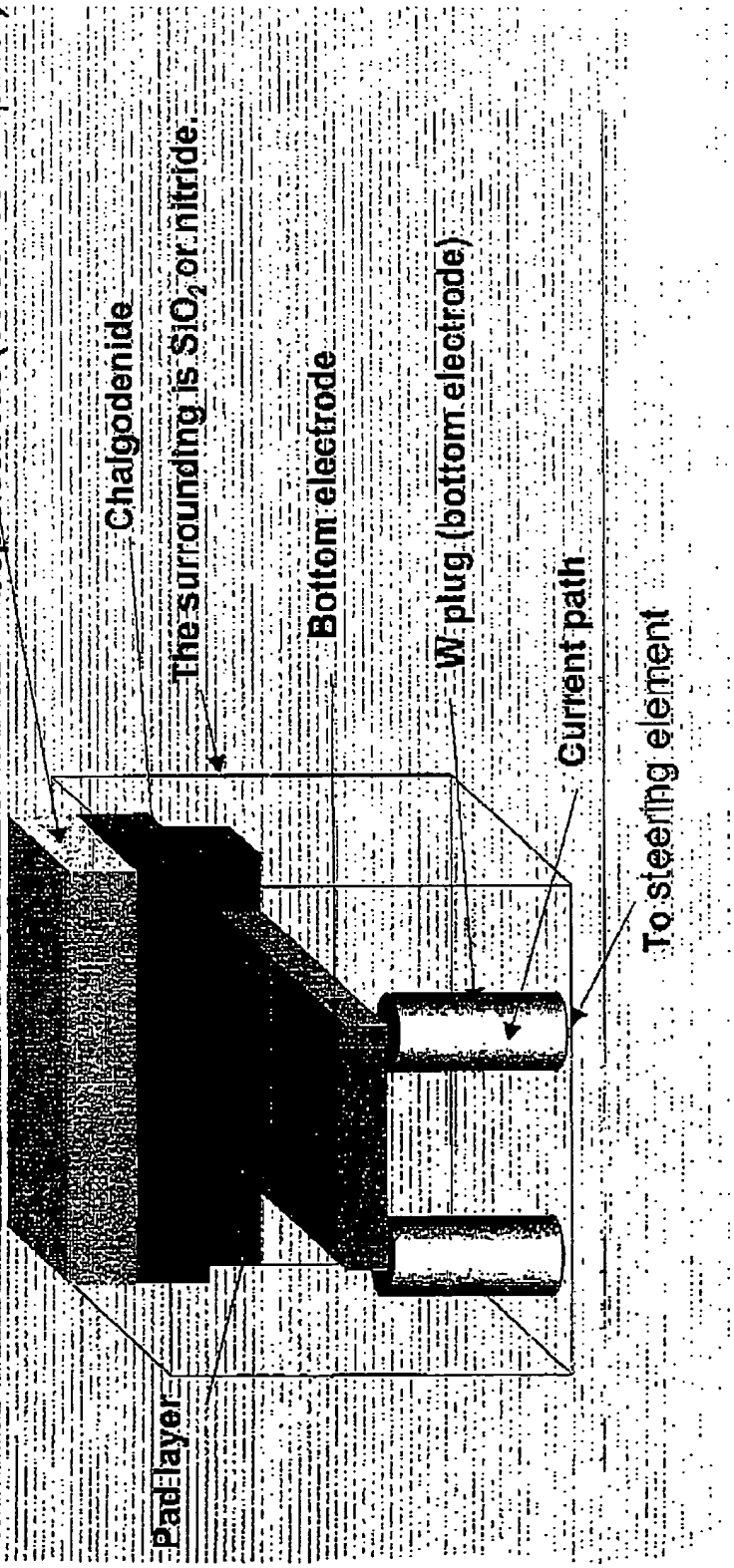
RELATED DRAWINGS

- A drawing of typical chalcogenide memory array.

BRIEF DESCRIPTION OF DRAWING

RELATED DRAWINGS

■ A model of the invention.



BRIEF DESCRIPTION OF DRAWING

RELATED DRAWINGS

- A model of the invention.

BRIEF DESCRIPTION OF DRAWING

RELATED DRAWINGS

- Process flow
- After regular CMOS process and W plug

AA' cross-section

Plan view (4 cells)

BRIEF DESCRIPTION OF DRAWING

RELATED DRAWINGS

- Pad layer (SLAB/PHOTO/ETCHING) Pad layer can be SiN, SiO2, or SiON etc...
- This process defines the height (h) of the bottom electrode.

AA' cross-section

Plan view (4 cells)

BRIEF DESCRIPTION OF DRAWING

RELATED DRAWINGS

- bottom electrode layer deposition (it can be TaN, TiN, TiW, Ti, W, poly or the combinations of above)

AA' cross-section

Plan view (4 cells)

BRIEF DESCRIPTION OF DRAWING

RELATED DRAWINGS

- Etching Back of bottom electrode
- Current and last processes define the width (w) of the chalcogenide part.

AA' cross-section

Plan view (4 cells)

BRIEF DESCRIPTION OF DRAWING

RELATED DRAWINGS

- Bottom electrode cutting(Photo/Etching)

AA' cross-section

Plan view (4 cells)

BRIEF DESCRIPTION OF DRAWING

RELATED DRAWINGS

- Cap layer Deposition (it can be SiON, SiO2, ZnS-SiO2, etc.)

AA' cross-section

Plan view (4 cells)

BRIEF DESCRIPTION OF DRAWING

RELATED DRAWINGS

- Routing1-Photo/Etching
- Etching process should cut the electrode again.
- This process defines length (l) of the bottom electrode

Plan view (4 cells)

AA' cross-section BB' cross-section

BRIEF DESCRIPTION OF DRAWING

RELATED DRAWINGS

- Routing2: Chalcogenide and top electrode dep/ Photo/Etching

Plan view (4 cells)

AA' cross-section BB' cross-section

PRIOR ART REFERENCE

	classific ation	Patent No	Title	Remark
Prior art-1	Patent	US6111264	Small pores defined by a disposable internal spacer for use in chalcogenide memories	Similar to US6189582
Prior art-2	Patent	US6031287	Contact structure and memory element incorporating the same	
Prior art-3	Patent	US6114713	Integrated circuit memory cell having a small active area and method of forming same	

•CATEGORY : ESSAY, PAPER, PATENT, PRODUCT ETC

COMPARING RELATED PRIOR ART WITH THIS INVENTION

	Disadvantages of the related Prior art	Differences from this invention
Prior art-1	1. Dielectric layer can reduce the pore size, but the shrinking ratio is not unlimited. Because overhang may seal the hole. Therefore, the pore size can be limited by lithography. It is difficult to scale down. 2. It's very difficult to control the size uniformity of ultra small pores with this method. 3. It's very difficult to place chalcogenide into the holes.	1. The current is limited by chalcogenide. 2. The minimal current path cross sectional area is defined by photolithin film/etching processes.

COMPARING RELATED PRIOR ART WITH THIS INVENTION

	Disadvantages of the related Prior art	Difference from this invention
Prior art 2	1. Electrode area can be reduced by this method, but the shrinking ratio is limited by the film thickness and photo. For example: if pore diameter is 0.15 um and film thickness is 200A, the shrinkage ratio is only about 50%. It is difficult to scale down. 2. Because the process needs to place electrode and oxide into small contacts, it is very difficult to process.	1. The bottom electrode is vertical and placed in a hole. 2. The crossectional area of chalcogenide is defined by photolithin film processes.

COMPARING RELATED PRIOR ART WITH THIS INVENTION

Prior art	Disadvantages of the related Prior art	Difference from this invention
Prior art 3	1. It is very difficult to control the electrode area	1. The cross-sectional area of chalcogenide is defined by photoetching processes

THE SCOPE OF THE PROTECTION OF THE PATENT

Main Feature of the Invention

- The contact area between the chalcogenide and electrode is defined by 1. electrode film thickness and 2. The thickness of pad layer. With well control of film thickness, the area will be very small. Therefore the current required in the chalcogenide phase-change memory is reduced.

The advantages of the invention

- Ultra small contact area between the chalcogenide and electrode.
- Easy to fabricate. (Do not need to place materials into small pores)
- Easy to scale down. (The scaling limit of thin film and etching is less than 50A in 0.25um technology.)
- Take an easy calculation as an example:

If the PAD layer thickness is 500A and the electrode layer thickness is 200A, which is easy to fabricate by 0.25um process, the contact area is less than 10^-8. This is the cross-section of a 0.036 um contact, which is almost impossible to fabricate nowadays.